68,700-016

FLEXIBLE MULTI-CHIP MODULE AND METHOD OF MAKING THE SAME

FIELD OF THE INVENTION

[0001] This invention relates to semiconductor packages, and more particularly to semiconductor packages involving flexible multi-chip modules and methods of making the same.

BACKGROUND OF INVENTION

[0002] A variety of semiconductor packages are known to those skilled in the art. Kondo, US Patent No. 6,469,903 states that it discloses a semiconductor device, including the flexible printed circuit having a first area part located in the center thereof, a second area part is provided continuous thereto, a third area part is provided continuous to the first part, and a wiring pattern formed on the surface of the above-described flexible circuit. A semiconductor element is mounted on a surface of the second part, and a second semiconductor element mounted on a surface of the third part. The second part is folded to a face side of a center part and a third part is folded to a rear side of the second part. However, Kondo teaches using a spacer in between chips that prevent the chips from engaging each other to provide group-packaging alignment. Therefore, in that disclosure, the physical implementation of packaging three chips requires three separate spacers, and each spacer require a bottom and top spot glassy epoxy to stick together.

[0003] Tesser, et al., US Patent No. 5,789,815 state that it discloses a three-dimensional package having a footprint size reduced by an approximate factor of four when compared to conventional electronic packaging. The module disclosed has a protective covering, such as a

cap or sealant, as a moisture barrier. Thus, high integration using flexible appendages attach to a rigid substrate and singularly folded above the substrate results in both a small footprint package and also a light package. A reel-to-reel flexible tape assembly provides pretested flex boards resulting in cost effective manufacturable package for semiconductor components. The disclosure teaches placing a microprocessor on the rigid substrate portion and semiconductor die on a flexible appendage, and the flexible appendage is folded over so that the semiconductor die overlap the microprocessor.

[0004] Nakatsuka, US Patent No. 6,208,521 discloses a semiconductor package having a central base portion with a semiconductor element mounted on the base portion and four flexible appendages extending from the base portion. Semiconductor elements are also attached on each of the flexible appendages and the flexible appendages are folded over so that they overlie the semiconductor element on the central base portion. An adhesive layer is provided to insulate the semiconductor element on the central base portion from the semiconductor element attached to one of the flexible appendages.

SUMMARY OF THE INVENTION

[0005] One embodiment of the invention includes a method of making a semiconductor package comprising: providing a semiconductor carrier comprising at least a first flexible appendage connected to the body portion; each flexible appendage having a top face and a bottom face; and the body portion having the top face and a bottom face, a first semiconductor device and a second semiconductor device, each having a front face and a back face, the first

semiconductor device and the second semiconductor device connected to the first flexible appendage with the front face of each semiconductor device facing the top face of the first flexible appendage, and forming a first fold in the first flexible appendage so that the back face of the first semiconductor device overlies the back face of the second semiconductor device.

[0006] Another embodiment of the invention includes a semiconductor package comprising a semiconductor carrier comprising at least a first flexible appendage connected to the body portion; each flexible appendage having a top face and a bottom face; and the body portion having the top face and a bottom face; a first semiconductor device and a second semiconductor device, each having a front face and a back face; the first semiconductor device and the second semiconductor device connected to the first flexible appendage with the front face of each semiconductor device facing the top face of the first flexible appendage and the first flexible appendage having a first fold therein so that the back face of the first semiconductor device overlies the back face of the second semiconductor device.

[0007] These and other embodiments of the present invention will become apparent from the following brief description of the drawings, detailed description of preferred embodiments and appended claims and drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] Figure 1 is a prospective view of a flexible multichip module according to one embodiment of the present invention.

[0009] Figure 2 is a prospective view of another embodiment of a flexible multichip module according to one embodiment of the present invention.

[00010] Figure 3 is an enlarged, sectional, partial view of a portion of a flexible multichip module according to one embodiment of the present invention.

[00011] Figure 4A illustrates an act in a method of making a flexible multichip module according to one embodiment of the present invention.

[00012] Figure 4B illustrates an act in a method of making a flexible multichip module according to one embodiment of the present invention.

[00013] Figure 4C illustrates an alternative act in a method of making a flexible multichip module according to one embodiment of the invention.

[00014] Figure 5 illustrates a flexible multichip module according to one embodiment of the present invention, having eight chips.

[00015] Figure 6 is an enlarged, sectional view of a portion of a flexible multichip module illustrating alignment keys on semiconductor devices of the flexible multichip module according to one embodiment of the present invention.

[00016] Figure 7A illustrates an act in a method of making a semiconductor device useful in making a flexible multichip module according to one embodiment of the present invention.

[00017] Figure 7B illustrates an act in a method of making a semiconductor device, having a key alignment feature thereon, useful in making a flexible multichip module according to one embodiment of the present invention.

[00018] Figure 7C illustrates an act in a method of making a semiconductor device with a second key alignment feature for making a flexible multichip module according to one embodiment of the present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[00019] Figure 1 illustrates one embodiment of a flexible multichip module according to the present invention in a laid open, unfolded position. The semiconductor package 10 includes a semiconductor device carrier 12, having a body portion 14. In one embodiment the carrier 12 comprises an anisotropic film having conductive particles that can be pressed and squeezed between a bump and wiring pattern by heating and pressing a semiconductor element and the film so that the bump and the wiring pattern are electrically connected. In another embodiment a wiring pattern may be provided in the carrier 12 exposed bond pads for making electrical connection to the carrier 12 in ways known to persons skilled in the art. In one embodiment, the body portion 14 is preferably flexible, made from a flexible material such as, but not limited to, a polyamide or other flexible circuit carrier known to those skilled in the art. The body portion 14

may also be rigid or semi-rigid made from a fiberboard base material, ceramic base material, plastic or other similar material. The body portion 14 includes a top face 16 and an opposite bottom face 18. The body portion 14 may include a first side 20 and an oppositely positioned second side 22 which in a preferred embodiment is parallel to the first side 20. The semiconductor package 10 includes a first flexible appendage 24, extending outwardly from the body portion 14. The first flexible appendage 24 includes a free end 26 and a second end 28 attached to the body portion 14. The first flexible appendage 24 includes a top face 30 and a oppositely positioned bottom face 32. The first flexible appendage 24 may include a first side 108 and an opposite second side 110. A first semiconductor device 34 is positioned on the first flexible appendage preferably near the free end 26. A second semiconductor device 36 is also positioned on the first flexible appendage 24 at a location nearer to the second end 28 of the flexible appendage.

[00020] The semiconductor package 10 may include an electrical connector 38 which, in one embodiment of the invention, extends from the body portion 14. The electrical connector 38 may include electrical leads or bond pads 40 thereon, so that the semiconductor package 10 may be electrically connected to external sources or devices.

[00021] In one embodiment, a second flexible appendage 44 may be provided and may extend from the body portion 14. The second flexible appendage may extend from the same side of the body portion or from an opposite side of the body portion 14. The second flexible appendage 44 includes a free end 46 and a second end 48 connected to the body portion 14. The

second flexible appendage 44 includes a top face 50 and an opposite bottom face 52. The second flexible appendage 44 may include a first side 112 and a opposite second side 114. Bond pads 42 may be provided on all of the flexible appendages to which semiconductor devices may be attached (as shown in Fig. 1).

[00022] In one embodiment, a third flexible appendage may be provided and extends from the body portion 14. In a preferred embodiment, the third flexible appendage extends from the same side of the body portion as does the first flexible appendage 24. The third flexible appendage 54 includes a free end 56 and a second end 58 attached to the body portion 14. The third flexible appendage 54 includes a top face 60 and an opposite bottom face 62, and a first side 116 and an opposite second side 118. Preferably, a first slot 86 is defined between the first flexible appendage 24 and the third flexible appendage 54.

[00023] In another embodiment, a fourth flexible appendage 64 may be provided, having a free end 66 and a second end 68 connected to the body portion 14. The fourth flexible appendage 64 includes a top face 70 and an opposite bottom face 72, and a first side 120 and an opposite second side 122. Preferably, a second slot 88 is provided between the second flexible appendage 44 and the fourth flexible appendage 64. Although the semiconductor package 10 shown in Figure 1 includes four flexible appendages, it will be appreciated that the semiconductor package may include numerous other flexible appendages by extending the body portion 14 in the direction of Arrow A and attaching a plurality of additional flexible appendages.

[00024] Referring now to Figure 2, it will be appreciated that a flexible multichip module, according to the present invention, may include a plurality of flexible appendages 24, 44, 54, 64 with several semiconductor chips attached to each flexible appendage. As shown in Figure 2, a first chip 34 and a second semiconductor chip 36 is attached to the first flexible appendage 24, and a third semiconductor chip 74 and a fourth semiconductor chip 76 is attached to the second flexible appendage 44. Similarly, a fifth semiconductor chip 78 and a sixth semiconductor chip 80 is attached to the third flexible appendage 54 and a semiconductor chip 82 and an eighth semiconductor chip 84 is attached to the fourth flexible appendage 64. Again, a slot 86 is defined between the first flexible appendage 24 and the third flexible appendage 54, and a slot 88 is defined between the second flexible appendage 44 and the fourth flexible appendage 64.

[00025] Referring now to Figure 3, in one embodiment, a first passive alignment key 90 is provided on one of the two chips on the same flexible appendage, and a second passive alignment key 92 on the other chip. Each chip may include a semiconductor substrate 94, having bond pads 96 formed therein or thereon, and a first passivation layer 98 overlying the semiconductor substrate with openings formed therein exposing a portion of bond pads 96. An electrically conductive bump 100 may be bonded to the bond pad 96. An electrical insulation layer 102 may optionally be formed over the backside of the semiconductor substrate 94. One of the semiconductor chips 34 includes the first passive alignment key 90 formed therein or thereon (preferably over the electrical insulation layer 102), and in this case, the key 90 is spaced a distance from the outer edge of the semiconductor substrate 94. The other semiconductor substrate 36 includes the second passive alignment key 92 formed over the backside of the

semiconductor substrate 94 and preferably on the electrical insulation layer 102. The second passive alignment key 92, in this case, is positioned near the outer edge of the semiconductor substrate 94. As will be appreciated as from Figure 1, in one embodiment, the first passive alignment key 90 is spaced a distance from the outer edge of the semiconductor chip, and in the embodiment shown in Figure 1, has a rectangular ring like shape. The second passive alignment key 92 is formed on the adjacent second chip 36 at a position near the outer edge of the semiconductor substrate, and in the embodiment shown in Figure 1, preferably has an "L" shape so that the first passive alignment key 90 may be mated with the second passive alignment key 92 to properly position the first semiconductor chip 34 over the second semiconductor chip 36 and so that the back face of each engage each other.

[00026] Referring again to Figure 1, a method of making a flexible multichip method according to the present invention includes forming a first fold, in the direction of the arrow labeled "Fold 1," in the first flexible appendage 24 so that the first semiconductor chip 34 overlies the second semiconductor chip 36. The alignment of the first semiconductor chip 34 to the second semiconductor chip 36 is aided by the first passive alignment key feature 90 on the first semiconductor chip 34 mating with the second passive alignment key 92 on the second semiconductor chip 36. Thereafter, the first flexible appendage 24 is folded again as shown by the arrow labeled "Fold 2" so that the bottom face 32 of the first flexible appendage 24 overlies, and preferably, engages the top face 16 of the body portion 14 as best shown in Figure 4a. In this arrangement, both the first semiconductor device 34 and the second semiconductor device 36 on the first flexible appendage 24, overlie the body portion 14. In another embodiment shown

in Fig. 4C, a semiconductor 200 may be secured to the body portion 14 and the first flexible appendage 24 is folded so the first and second semiconductor devices 34 and 36 overlie the semiconductor 200 on the body portion 14.

[00027] Referring again to Figure 1, the second flexible appendage 44 may be folded a first time as shown by fold arrow labeled "Fold 3" so that the third semiconductor chip 74 overlies and engages the fourth semiconductor chip 76 using the alignment keys 90, 92 on both chips. The second flexible appendage 44 is folded a second time as illustrated by the arrow labeled "Fold 4" so that a portion of the bottom face 52 of the second flexible appendage 44 overlies, and preferably, engages a portion of the bottom face 18 of the first flexible appendage 24 so that the third semiconductor chip 74 overlies and is nearest the second semiconductor chip 36 on the first flexible appendage 24, as will be best seen from Figure 4b.

[00028] The third flexible appendage 54 may be folded in the manner similar to the first flexible appendage 24 so that a first fold is formed in a manner illustrated by the arrow labeled "Fold 5" so that the fifth semiconductor chip 78 overlies and is aligned preferably by the keys 90, 92 with semiconductor chip 68 on the third flexible appendage 54. The third flexible appendage 54 is then folded a second time as illustrated by the arrow labeled "Fold 6" so that the bottom face 62 of the third flexible appendage 54 overlies and engages a portion of the top surface 16 of the body portion 14. In this arrangement, the fifth semiconductor chip 78 is nearest the body portion 14.

[00029] The fourth flexible appendage 64 may be folded in a manner similar to the second flexible appendage 44 including folding the fourth flexible appendage 64 a first time as illustrated by the arrow labeled "Fold 7" so that the seventh semiconductor chip 82 is overlying, aligned and engaged with the eight semiconductor chip 84 on the fourth flexible appendage 64. The fourth flexible appendage 64 is then folded a second time as illustrated by the arrow labeled "Fold 8" so that a portion of the bottom face 72 of the fourth flexible appendage 64 overlies and engages a portion of the bottom face 62 of the third flexible appendage 54. In this arrangement, the seventh semiconductor chip 82 overlies and is nearest the sixth semiconductor chip 80 on the third flexible appendage 54. Alternatively, an adhesive layer 106 may be interposed between folded sections of appendages as will be best appreciated by Figure 4b.

[00030] In another embodiment of the invention, the body portion 14 may be folded in a direction as shown by arrow labeled "Fold 9" to form a semiconductor package with the eight semiconductor chips 34, 36, 74, 76, 78, 80, 82, 84 stacked on top of each other. A flexible multichip module with eight semiconductor chips stacked on top of each other according to the present invention is illustrated in Figure 5.

[00031] Referring now to Figure 7a, a semiconductor package according to the present invention may be made by providing a first semiconductor device 34, including a substrate portion 94 and bond pads 96 formed thereon or therein, and a first passivation layer 96 formed over the substrate portion and having openings formed therein each exposing a portion of a bond pad 96. An electrical insulation layer 102 may be deposited on the back face of the substrate

portion, and a first passive alignment key 90 may be formed on the semiconductor device 34 directly on the substrate portion 94 or over the electrical insulation layer 102 (if present), as shown in Figure 7b. A second semiconductor device 36 may be provided, also having a substrate portion 94, bond pads 96 formed thereon or therein, a first passivation layer over the substrate portion having openings therein, each exposing a portion of a bond pad 96. Optionally, the second semiconductor device 36 may include an electrical insulation layer 102 overlying the backside of the substrate portion 94. A second alignment key 92 may be formed directly on the substrate portion 94, or on the electrically insulation layer 102 if present. In a preferred embodiment, the first passive alignment key 90 and the second passive alignment key 92 have configurations as illustrated in Figure 1.